Suresh Kumar
Email: sanam.sureshkumar93@gmail.com
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Business focused Technical with 5.2 years in Development activities for Embedded Systems, Boot Support Packaging & RTOS, and Storage Domains.

Professional summary:

- Hands on with User space (applications), Kernel Space (Drivers) Development, Board Bring up, Bare-metal Software for making the U-boot, Kernel active.
- Hands on NAND Flash, Storage SSD & HDD Testing.
- Hands on tools - Jira's, GIT, SVN & Jenkins Tools, Debugging with Trace-32 –Lauterbach, ARM DS5 debuggers.
- Hands on Evaluation boards Raspberry-pi, Beagle bone black, Xilinx Zynq Boards, RISC-V (Freedom usdk unleashed boards).
- Hands on Embedded Micro Controller based Product chip design etc., for IOT platforms
- Hands on Experience in IPC Mechanisms, multi-threaded applications, Socket programming, Character driver & DMA application changes.

Technical, Functional & Managerial:

Programming : C
OS: Linux (Ubuntu, Centos), XRS.
Protocols: I2C, UART, PCI & USB, TCP/IP.
Software Development, Testing, Root Cause Analysis, Release Documentation

Work Experience

May'18-Till date: Adept chips as Firmware Lead Engineer

- Implementing Bare Metal code for IP driver Peripherals Validation like UART, GPIO, DMA, NVIC Bare metal driver code & test applications.
- Working on BSP Code Integration and debugging activities. Checking the register level access for every driver IP peripherals for Read/Write access.
- Working on writing Linux applications for camera related projects for virtual reality based. Host pc to client pc communication through TCP/IP protocol and socket programming activities.

Oct'17-Feb'18: Western Digital Corporation as Member Technical Staff Engineer

- Worked with Brisa Technologies payroll.
- Worked on Software Product Integration for NAND flashes SOC.
- Worked on C coding BUG Fixing Activities for Testing the ARM a53 based SOC kit Multi Core Architecture designed products for customers.
- Debugging activities for manufacturing firmware of SSD drives host (PCI-NVMe) & host less (PCI-USB) boards for U2 and M2 drives.
- Worked on Niagara Testing Tool and fix the issues with Memory Maturity Tool for host based environment.

July'16-July'17: Moschip semiconductors as Firmware Senior engineer

- Worked on Linux SOC platforms like ARM1176, ARM Cortex-A9 based SOC Kit.
- Worked on U-Boot, Kernel Related Issues as a part of Board Bring-up activities.
- Working on u-boot Peripheral porting issues. Make the ports enable or disable as per the requirements

June'14-April'16: Seagate technology (HDD) India Pvt ltd. as Firmware engineer

- -Worked in Clogeny Technologies from june-14 to june-15 and moved to seagate as a part of acquisition.

- Developed XRS (Customized OS) for Seagate hardware platforms, developing kernel level drivers, testing them to their suitability for Seagate products.
- Worked on Enclosure Management, BMC (Base management controller), and Mellanox devices for test automation activities in Build and Integration Role.
- Worked on RTOS Platform to Test multiple Drives booting sequence in various platforms.

Educational details

- Master of technical education (Electronics & Communication) from Geetanjali College of Engineering & Technology- JNTUH.
- Bachelor of technical education (Embedded Systems) from Sree Visveswaraya Institute of Technology- JNTUH.

Project Details:

Project 1: Sifive Evaluation Board Bring up and IP peripherals Feature Enhancement for U540 board through freedom-sdk Setup.

Role: Firmware Lead engineer

Description: Project Scope is based on RISCV open source architecture specific development of device driver development activity.

- UART device driver bringup and feature enhancement activity work in progress.
- USB activity for files transfer required packages like xmodem, Kermit process of file transfer device and host side activities is done.

Project 2: Stream Network for Camera display system for TCP/IP Client Server protocol using Socket programming.

Role: Firmware engineer

Description: Project is based on xilinx zcu102 Evaluation board platform, DSI firmware application development for Remote PC to Host FPGA-1 TX and RX FPGA-2 to Client PC.

Host PC to FPGA Board-1: Application on host side will send the data received from DSC software to FPGA board-1 through Ethernet Windows PC, Ethernet receives the data and store it in SD card as a file in .dsc format, the .dsc file will be further transferred to the ddr by filling the DMA buffer, and then data will be transferred to the TX DSI.

FPGA Board-2 to Client PC: RX DSI will receive the data in .dsc format and once after receiving firmware will transfer it to the ddr and then to SD card, .dsc file stored in SD card will be transferred to Client PC through Ethernet.

Integrating the firmware in Linux environment with the application running in windows environment for communication using socket.

Project 3: Bare Metal code development activity for Virtual Reality with ARM cortex M33 processor.

Role: Firmware Lead Engineer

Description: Bare Metal code for IP driver Peripherals Validation like uart, gpio, axi_dma, ahb_dma and nvic device driver code & test applications as per the product functionalities- Worked in polled and interrupt modes.

- Worked with Pulse width Modulation (pwm) device driver to check the high time and period time.
- Worked with Triple timer counter (ttc) device driver to check free running, overflow with match, interval with match mode, Event timer modes.
- Worked with gpio & misc module device driver code to write and read to the I/O ports, port to port connectivity.
- Worked with dma (axi, ahb) to check the bus, channels connectivity, buffer filling activity.
- Worked with nvic driver activity to simulate irq's, Software trigger interrupt, nvic-uart test activity.

Project 4: Stream TV Network based Display management system

Role: Firmware Lead Engineer

Description: This is a terminal board based on multicore SoC, meant to collect data from array of cameras (SLAM, Eye tracker and RGB etc.), array of MiCs'. It is required to aggregate camera and MiC data and send to host using USB or Interlaken. This is meant for high end AR/VR terminal, it is generic enough to be used for Autonomous cars.it is having sensor hub as well to host multiple sensors Major functionalities - Components of Terminal. There are 4 major functional blocks of Terminal.

- Camera Hub – Having multiple types of cameras
- Sensor Hub- To connect various sensors.
- Audio Processing and Ios.
- Connectivity to Host.

Project 5: NAND flashing for multicore processor on arm cortex-a9, a53 etc., based SSD.
Role: Member Technical Staff Engineer
Description: Project is based on multicore architecture based on arm cortex-a9, a53 and Atmel the Objective is to write a user space application on board with nand flashing and writing api application to read and display the info.

- Transition diagnostics team which measures the NAND info of read, write, erase bad block management and to re correct the data.
- To check the asic wafers, nand wafers, capacitor check etc.,

Project 6: U-boot porting on ARM cortex-A9, ARM 1176 Anurag SOC boards.
Role: Firmware senior engineer
Description: Project is based on U-boot validation of peripherals (Ethernet, GPIO, UART, SPI, KMI, I2C etc.,) with ARM Cortex-a9 based.

- Worked on C coding bug fixing activities for Pre and Post Silicon Validation activities for IP peripheral validation etc.,
- Virtex-7 FPGA on the board, connected to zynq 7000.
- NIC 300 bus interface connects these block peripheral.
- To write IP peripheral driver, test application, unit test cases for Target FPGA platform.

Project 7: Booting Support for real time operating systems in Storage (Servers) & Automation Tests Performed
Role: Firmware Engineer
Description: The project deals with the installation checking whether the correct kernel, RPM, release Version, correct selected drive installed, drive is cleaned, swap disk sizes for the whole test analysis report, creating documentations of this procedure to check OS is installed correctly into the drive

- The involved understanding and modifications of scripts in python for automating command line (cli) parameters for installation check & create report,
- To create log whether the installation performed on the drives are correct.
- No of types of installations along with bugs issue creating new Jira tasks for resolving the issues.

Personal Details:
Date of Birth: 8 June 1990
Marital status: Married
Bangalore.